IN THE CLAIMS:

Please amend the claims as follows:

Claim 1 (Currently Amended): ~~A method for~~ An accessing method of a frame memory integrated within a display panel driver driving a display panel driven by a sub-field addressing method in which one frame of video data is divided into P sub-fields each consisting of N pixel lines and each of said of N pixel lines having a pixel data set, said accessing method comprising:

~~serially~~ performing a plurality of write operations for sequentially writing ~~sub-field data of a pixel line within said display panel for~~ a plurality of ~~sub-fields~~ pixel data sets into said frame memory such that pixel data sets on m-th line ($1 \leq m \leq N-1$) are sequentially written in order of said P sub-fields from a first sub-field to a last sub-field, and then when a pixel data set at said last sub-field has been written, pixel data sets on (m+1)-th line are sequentially written in order of said P sub-fields from a first sub-field to a last sub-field; and

~~serially~~ performing a plurality of read operations for sequentially reading ~~sub-field data of~~ a plurality of ~~pixel lines for a sub-field~~ pixel data sets from said frame memory such that pixel data sets on q-th sub-field ($1 \leq q \leq P-1$) are sequentially read in order of said N pixel lines from a first pixel line to a last pixel line, and then when a pixel data set at said last pixel line has been read, pixel data sets on (p+1)-th sub-field are sequentially read in order of said N pixel lines from a first pixel line to a last pixel line,

wherein at least two of said write operations are allowed to be performed between adjacent two of said read operations.

Claim 2 (Original): The method according to claim 1, further comprising:

providing first and second horizontal sync signals,

wherein said write operations for writing said sub-field data of said pixel line for said plurality of sub-fields are performed during a single cycle of said first horizontal sync signal, and

wherein each of said read operations for reading said sub-field data of said pixel line for each of said plurality of sub-fields is performed during a single cycle of said second horizontal sync signal.

Claim 3 (Original): The method according to claim 1, further comprising:

providing a read request signal activated for requesting said read operations, and

providing a write request signal activated for requesting said write operations,

wherein, in response to activation of said read request signal, associated one of said read operations is performed immediately after said activation of said read request signal when said frame memory is not engaged in write operation, while said associated one of said read operations is performed after completion of associated one of said write operations when said frame memory is engaged in said associated one of said write operations.

Claim 4 (Original): The method according to claim 3, wherein said read request signal is kept activated until said associated one of said read operations is initiated.

Claim 5 (Original): The method according to claim 1, further comprising:

providing a read request signal activated for requesting said read operations, and

providing a write request signal activated for requesting said write operations,

wherein, in response to activation of said write request signal, one of said write operations associated with said activation is performed immediately after said activation of said write request signal when said frame memory is not engaged in read nor write operation, said associated one of said write operations is performed after completion of associated one of said read operations when said frame memory is engaged in said associated one of said read operations, and said associated one of said write operations is performed after completion of previous one of said write operations when said frame memory is engaged in said previous one of said write operations.

Claim 6 (Original): The method according to claim 5, wherein said write request signal is kept activated until said associated one of said write operations is initiated.

Claim 7 (Currently Amended): A memory controller for controlling access to a frame memory integrated within a display panel driver driving a display panel driven by a sub-field addressing method in which one frame of video data is divided into P sub-fields each consisting of N pixel lines and each of said of N pixel lines having a pixel data set, said frame memory being accessed via a plurality of write operations for sequentially writing a plurality of pixel data sets into said frame memory such that pixel data sets on m-th line ($1 \leq m \leq N-1$) are sequentially written in order of said P sub-fields from a first sub-field to a last sub-field, and then when a

pixel data set at said last sub-field has been written, pixel data sets on (m+1)-th line are sequentially written in order of said P sub-fields from a first sub-field to a last sub-field, and via a plurality of read operations for sequentially reading a plurality of pixel data sets from said frame memory such that pixel data sets on q-th sub-field ($1 \leq q \leq P-1$) are sequentially read in order of said N pixel lines from a first pixel line to a last pixel line, and then when a pixel data set at said last pixel line has been read, pixel data sets on (p+1)-th sub-field are sequentially read in order of said N pixel lines from a first pixel line to a last pixel line, said memory controller comprising:

a timing controller developing read and write start pulse signals in response to write and read request signals, and

a read/write operation control unit responsive to said read and write start pulse signals for initiating read operations for reading sub-field data from said frame memory, and write operations for write sub-field data into said frame memory,

wherein said timing controller develops said read and write start pulse signals to allow said read/write operation control unit to initiate at least two of said write operations between adjacent two of said read operations.

Claim 8 (Original): The memory controller according to claim 7, wherein said timing controller includes:

a state machine switching a state of said frame memory among a plurality of states in response to a reset signal, said write and read request signals, said plurality of states comprising:

an idle state,

a write start state,

a first write operation state, and

a second write operation state,

wherein said state machine is designed to switch said state of said frame memory to said idle state in response to activation of said reset signal, to switch said state of said frame memory to said write start state in response to first activation of said write request signal, to unconditionally switch said state of said frame memory to said first write operation state after placing said frame memory in said write start state to initiate one of said write operations, and to switch said state of said frame memory to said second write operation state in response to second activation of said write request signal during said one of said write operations to initiate next one of said write operations.

Claim 9 (Original): The memory controller according to claim 8, wherein said plurality of states further comprising:

a read start state, and

a read operation state,

wherein said state machine is designed to switch said state of said read start state in response to activation of said read request signal when said frame memory is placed in any of said idle state and said first and second write operation states, and to unconditionally switch said state of said frame memory to said read operation state after placing said frame memory in said read start state to initiate one of said read operations.